A new PieceWiseLinear (PWL) function is proposed for the decoding of the Low-Density-Parity-Check (LDPC) code with the Self Adjustable Offset Min-Sum (SAOMS) algorithm. Avoiding the use of the non-linear function $f(x) = \ln \left( \frac{1}{1 + e^{-2x}} \right)$ in the adjustable offset factor, this linear approximation greatly simplifies the hardware implementation with a little BER performance loss. The proposed solution is new, useful and is successfully tested on decoding regulars (504, 252) and (8000, 4000) LDPC codes. The corresponding Check Node Processing Unit (CNPU) have been designed, described and simulated using Very High Speed integrated circuits Hardware Description language (VHDL). The synthesis results were obtained using an Altera Quartus II software with cyclone II EP2CF896C6 as the target FPGA device. The designed CNPU is fully parallel and flexible to be used for different block length when a regulars (3, 6) LDPC codes are required.

References


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**Index Terms**

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LDPC  BER  FPGA  BP  PWL  VHDLifx