Abstract

This paper describes three techniques for controlling the loop filter of the PLL for high operating speed. The proposed fast-locking PLL reduces the pull-in time and enhances the switching speed, while maintaining better noise bandwidth. Extended loop bandwidth enhancement is achieved by the adaptive control on the loop filter resistances. This work differs from previously published results in that it presents a comprehensive study for modeling, circuit simulation and practical circuit implementation of a 2nd order PLL with loop filter control for speeding-up the PLL. The overall improvement in performance of the proposed PLL is evaluated and compared with the conventional PLL. An industrial CMOS IC is used to implement the PLL.

References


Index Terms

Computer Science  Circuits And Systems
Keywords
Phase locked loop  speeding-up  adaptive bandwidth  natural frequency  settling time