Area and Power Efficient CMOS Adder Design by Hybridizing PTL and GDI Technique

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Abstract

In this paper an area and power efficient 9T adder design has been presented by hybridizing PTL and GDI techniques. The proposed adder design consist of 5 NMOS and 4 PMOS. A PTL based 5T XOR-XNOR module has been proposed to improve area at 120 nm and 90nm technology and compared with the previous XOR-XNOR design. The proposed Hybrid full adder design is based on this area efficient 5T XOR-XNOR module design. To improve area and power efficiency a cascade implementation of XOR module has been avoided in the proposed full adder. XOR-XNOR modules outputs act as input to Carry and Sum module which has been implemented by the GDI MUX. The proposed adder has been designed and simulated using DSCH 3.1 and Microwind 3.1 on 120nm and 65nm technology. Also the simulation of layout and parametric analysis has been done for the proposed full adder design. Power and current variation with respect to the supply voltage and temperature has been performed on BSIM-4 and LEVEL-3 on 120nm. Results show that area consumed by the proposed hybrid adder is 98.5µm² on 120nm technology. At 1.2V input supply voltage the proposed adder has shown an improvement of 76.9% in power and 74.82% in current on BSIM-4 120nm technology.
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**Index Terms**

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**Keywords**

BSIM  
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Gate Diffusion Input  
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