Abstract

VLSI testing has been an essential part of chip design recently. A circuit must be tested before fabricating to avoid any malfunctioning. Testing a circuit has become mandatory that the circuit must be designed by ensuring testability. In VLSI testing, the circuit for testing is embedded with the actual design itself to reduce area and it is known to be Built-In Self Test (BIST). The test patterns generated by BIST are applied to the circuit. The test patterns are to be optimized to cover all the faults, reduce testing time and consume less power. This is achieved by employing Evolutionary Algorithms in selecting the patterns such that the inputs of design switch minimally. Test pattern generator is designed using these evolutionary algorithms so that the test vectors selected can be used for reducing the switching activity in the circuit and also by maintain the fault coverage. Genetic Algorithm and Particle Swarm Optimization are concentrated and their efficiencies are explained in this work.

References

- F Corno, M Rebaudengo, M Reorda, G Squillero and M Violante, "Low Power BIST via Non-Linear Hybrid Cellular Automata," Proceedings of VLSI Test Symposium
Evolutionary Algorithms for Low Power Test Pattern Generator

(VTS'00), pp. 29 – 34, 2000.

- Dhiraj Sangwan, Seema Verma and Rajesh Kumar, "A Genetic Algorithm based Two Phase Fault Simulator for Sequential Circuit", International Journal of Computer...
Evolutionary Algorithms for Low Power Test Pattern Generator


Index Terms
Computer Science
Circuits And Systems

Keywords
Evolutionary algorithms Genetic Algorithm Particle Swarm optimization Low power Test Pattern Generation