Abstract

Today, at the low end of the communication protocols we find two worldwide standards: I2C and SPI [7]. I2C – commonly known as Inter IC, is a bus protocol. I2C protocol was proposed by Philips Semiconductors to enable faster device to communicate with slower devices without any data loss [1]. In this paper, we will assist the system designers to understand the communication between EEPROM (24C02) and FPGA Spartan 3A. The design is synthesized and simulated using Xilinx ISE and 7.1 and 12.4. Programmed FPGA acts as a master where as EEPROM acts as a Slave.

References

- Kangshun Li1,2, Yan Chen1 and Hezuan Liu2. A New Method of Evolving Hardware Design Based on IIC Bus and AT24C02. Proceedings of the 10th World Congress on Intelligent
Control and Automation July 6-8, 2012, Beijing, China
- ST24C02, user manual by ST MICROELECTRONICS

**Index Terms**

Computer Science  
Integrated Circuits

**Keywords**

FPGA  I2C Bus  Verilog