Abstract

Today, at the low end of the communication protocols we find two worldwide standards: I2C and SPI [7]. I2C – commonly known as Inter IC, is a bus protocol. I2C protocol was proposed by Philips Semiconductors to enable faster device to communicate with slower devices without any data loss [1]. In this paper, we will assist the system designers to understand the communication between EEPROM (24C02) and FPGA Spartan 3A. The design is synthesized and simulated using Xilinx ISE and 7.1 and 12.4. Programmed FPGA acts as a master where as EEPROM acts as a Slave.

References

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Keywords
FPGA  I2C Bus  Verilog