In Integrated circuits a gargantuan portion of on chip power is expended by clocking systems, which comprises of timing elements such as flip-flops, latches and clock distribution network. These elements absorb approximately 30% to 60% of the total power dissipation in the system. In order to design high performance and power efficient circuits a scrupulous approach should be adopted to reduce the power consumed by flip-flops and latches. In this paper various power efficient flip-flops with low power clock distribution network are examined. Among these flip-flops low Power Clocked Pass Transistor Flip-Flop (LCPTFF) consumes least power than Clocked Pair Shared Flip-Flop (CPSFF), Conditional Data Mapping Flip-Flop and Conditional Discharge Flip-Flop (CDFF). We propose a novel Low Power Forced Stack Clocked Pass Transistor Flip-Flop (LP-FSCPTFF) which reduces the power consumption by approximately 30.
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1% to 83.93% at 500MHz and 25.5% to 90.1% at 750MHz as compared to original LCPTFF. The simulation is carried out on Tanner EDA v13.0 at 90nm on different voltages at 500MHz and 750MHz. The temperature variation of different flip-flops is also shown at 5 °C, 25 °C and 50 °C.

References

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