Hybrid Cache Coherence Protocol for Multi-Core Processor Architecture

Abstract

The advances in circuit technology with constraints in power dissipation and clocking have led to integrating more processing cores onto a single chip, making it as the dominant processor architecture. This design of multi-core architectures also referred to as Chip Multiprocessors (CMPs) are gaining popularity because they have the potential to drive the future performance gains without any problems of power dissipation and complexity. Nevertheless, in order to run several independent programs in different processing cores requires them to cooperate for a single computation. Thus the communication architecture is the primary focus of research in achieving the scalability of this architecture. Coherence protocols and interconnection networks have resolved some communication gaps, but memory communication through cache has been the focus of attention in CMP. This problem has been addressed with many hardware and software solutions like Directory-based, Snoopy-based, Snarfing, etc., but the performance of the system is still not up to the level of expectation. The proposed model is to develop a hybrid cache coherence protocol referred as MESCIF (Modified Exclusive Shared Clean Invalid Forward), which combines the advantages of both directory-based and broadcasting protocols. This can be achieved by introducing a small directory based cache (DB-CACHE) and cache-coherence bus (CC-BUS) into the existing CMP architecture which overcomes the problems of existing methods. The architecture is simulated using a modular discrete event
driven computer system simulator platform called gem5 simulation tool.

References

- Gem5 simulator: http://www.m5sim.org.

Index Terms

Computer Science Communication Systems

Keywords

Cache Coherence Directory Based Cache Chip Multiprocessor Gem5 simulator