Abstract

In this paper revolves around the design and implementation of Carry Skip BCD adder using reversible logic to improve the design in terms of the number of garbage outputs and the number of gates used. In recent years, reversible logic has emerged as a promising technology having its applications in low power CMOS, quantum computing, nanotechnology and optical computing because of its zero power dissipation under ideal conditions. In this paper, the reversible logic implementation of Carry skip BCD adder is done so as to minimize the number of gates used and their garbage outputs. The existing and the proposed Carry skip BCD adders are designed using Verilog and simulated using Xilinx ISE 9.1i tool.

References

A Novel Design of Carry Skip BCD Adder using Reversible Gates

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Index Terms
- Computer Science
- Circuit And Systems

Keywords
- Reversible Gate
- Garbage Outputs
- Constant inputs
- Quantum Cost