Abstract

Among the assorted logic styles used in fostering the integrated circuits, the domino logic styles offers higher speed and smaller transistor count as compared to the static cmos circuits. However the domino logic suffers from lower noise immunity and higher power dissipation due to the problem of charge sharing and sub-threshold leakage currents. In this paper some of the earlier proposed techniques to reduce the power consumption of the domino circuits like Dual threshold voltage (DTV) and Dual threshold voltage—voltage scaling (DTV-S) have been analyzed. A novel stacked transistors Dual threshold voltage (ST-DTV) approach which deploys DTV technique with stacked transistors together with a voltage regulated static keeper
is analyzed to abate the total power dissipation of the circuit together with a better Power delay product (PDP). The ST-DTV design is tested on a 3-input OR gate and a 4x1 multiplexer at 90nm technology on multiple voltages and frequencies. Tanner tool EDA v13.0 is used for simulation.

References


Index Terms

Computer Science
Electronics
Keywords
  Domino logic  dual threshold voltage  voltage Scaling.