Abstract

The evaluation of integrated circuits such as Phase Locked Loops is a challenge in mixed-signal design. In most cases, these circuits are evaluated with electrical stimulations. To verify the proper operation of system before moving on to the design process, it is necessary to model these performances parameters with a hardware description language. At behavioral level, the performances of circuits are optimized without considering its transistor level structure. This paper, present an exact s-domain model analysis of a Third-Order Charge-Pump Phase-Locked Loops (CP-PLLs) used for wireless sensor transceiver using state equations of Phase Frequency Detector. Both the state equations and the transfer functions behavior modeling are described using this analysis. The linear state equations and s-domain transfer functions are provided. Critical advantage of illustrated methodology is a shortened PLL operating process due to the use of fast-simulating models at behavioral level. The analysis is verified using behavioral simulations with VHDL-AMS in Simplorer.
- K. Holladay, Design a PLL for specific loop bandwidth, END EUROPE, pp 64-66,
October 2000.


**Index Terms**

| Computer Science | Wireless |

**Keywords**

CP-PLLs  State Equations  S-Domain Model  Behavior Modeling  VHDL-AMS.