Abstract

This paper explains the performance analysis of Gate-All-Around silicon nanowire with 80nm diameter field effect transistor based CMOS based device utilizing the 45-nm technology. Simulation and analysis of nanowire (NW) CMOS inverter show that there is the reduction of 70% in leakage power and delay minimization of 25% as compared with 180 nm channel length. Gate-All-Around (GAA) configuration provides better and low drain induced barrier lowering (DIBL) ~63. 3mV/V and competent Subthresold slope ~95mV/V. GAA achieved the better voltage gain of ~10. 1 V/V. Static noise margin improved with 400mv. It provides high on drive current ~6mA this is validated that the threshold voltage of GAA field effect transistor.

References


**Index Terms**

Computer Science  
Circuits And Systems

**Keywords**  
Gate-All-Around (GAA); silicon nanowire; Drain induced barrier lowering (DIBL); Metal oxide semiconductor field effect transistor (MOSFET)