Abstract

The multiplication and accumulation are the vital operations involved in almost all the Digital Signal Processing applications. Consequently, there is a demand for high speed processors having dedicated hardware to enhance the speed with which these multiplications and accumulations are performed. In the present conventional circuits, the multiply accumulate unit multiplies the two operands, adds the product to the previously accumulated result and stores back the new result in the accumulator all in a single clock cycle. On the other hand, using reversible logic the implementation of digital circuits is gaining popularity with the arrival of quantum computing and reversible logic. In this paper, a novel reversible multiply accumulate unit is proposed. the comparison of various possible implementations of the reversible multiply accumulate unit in terms of gate count, quantum cost, constant inputs and number of garbage outputs is carried out.
Design of Efficient Reversible Multiply Accumulate (MAC) Unit

- Matthew Morrison and Nagarajan Ranganathan, &quot;Design of a Moore Finite State Machine using a Novel Reversible Logic Gate, Decoder and Synchronous Up-Counter,&quot; Proceedings of the Eleventh IEEE International Conference on Nanotechnology, pp.
Design of Efficient Reversible Multiply Accumulate (MAC) Unit


Index Terms
Computer Science
Circuits And Systems

Keywords
Reversible Multiply Accumulate Unit
Digital Signal Processors
Reversible Shift
Register
Reversible Adder
Reversible Multiplier
Quantum Cost.