Abstract

Multiplication is an operation much needed in Digital Signal Processing for various applications. This paper puts forward a high speed Vedic multiplier which is efficient in terms of speed, making use of Urdhva Tiryagbhyam, a sutra from Vedic Math for multiplication and Kogge Stone algorithm for performing addition of partial products and also compares it with the characteristics of existing respective algorithms. The below two algorithms aids to parallel generation of partial products and faster carry generation respectively, leading to better performance. The code is written in Verilog HDL and implemented on Xilinx Spartan 3 and Spartan 6 FPGA kit using Xilinx ISE 9.1i. The propagation delay of the implemented architecture is obtained to be 28.699ns and 15.752ns respectively.
Design and FPGA Implementation of High Speed Vedic Multiplier

Varanasi, India.

Index Terms

Computer Science Circuits And Systems

Keywords

VM-Vedic Multiplier KSA-Kogge Stone Adder RCA-Ripple Carry adder
CLA-Carry look-ahead Adder
CSA-Carry Save Adder.