Abstract

The demand for satellite communication and a wide-ranging objective, however, is often to achieve maximum data transfer, in a minimum bandwidth while maintaining an satisfactory quality of transmission. The transmission quality is basically concerned with the probability of bit error at the receiver here with respect to communication. This is an attempt to achieve highest capacity with minimum error rate by implementing modern codes named as LDPC (Low Density Parity Check codes) and it is represented here various decoding schema to decode and encode them. At the present time LDPC codes has received a superior interest because their error correction performance and their functional world wide applications. The paper represents LDPC significance, its characteristics and encoding and iterative decoding approaches to achieve channel capacity. Thus we need some technology that utilizes this available bandwidth by providing good error correction capability. We can also achieve it by using FPGA spartan 3e's VHLD implementation.

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Index Terms

Computer Science
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Keywords
Bit Error Rate
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parity check codes
Bit Flipping
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