Abstract

The fast growth of the power density in integrated circuits has made area and power dissipation as the vital design measures. In this paper, several different flip-flop topologies are analyzed and an area, power efficient flip-flop design is proposed. This design overcomes the power dissipation due to the large precharge node capacitance, with reduced number of transistors. The comparative power analysis and performance improvements indicate that the proposed design is suitable for high-performance digital designs where the area and power dissipation is of major concern. The simulation results are verified using tanner v7.0 tool. The performance comparisons are made using CMOS 0.18µm technology.

References

A Novel Analysis on Low-Power High-Performance Flip-Flops


Index Terms

Computer Science
Circuits And Systems

Keywords

Precharge node capacitance  power dissipation  high-performance