Abstract

Power reduction in electronic and computing system is one of the basic requirements and is increasingly demanded for the battery operated mobile systems. Although the power is required for every part of the system but the devices accessed most frequently (processor, DRAM) are taken special attention, because the improvement in power dissipation in these devices can dramatically reduce the overall power requirement. Since the many approaches have been already proposed for the power reduction in processor this paper focuses on the power reduction in DRAM. The DRAM may be considered as most power consuming device after processor, even when it is idle. Although the DRAMs inherently supports different power saving modes, like self-refresh and power-down, but these techniques are not as efficient and also causes the unwanted delay which in non-compensable for the many multimedia applications. Hence in this paper, we propose and evaluate an efficient DRAM rank grouping and power gating technique for power-saving that optimizes the power saving with marginal performance degradation. The proposed approach is developed and tested on several multimedia operations and the experimental results show that it reduces the total DRAM energy consumption between 56% and 183%(approx)at a negligible performance penalty between 3%
and 5\%(approx).

References

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Index Terms

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Keywords

Group-based Power Saving  Power Gating  and DRAM-Memory