Binary addition is a fundamental operation in most digital circuits. There are a variety of adders, each has certain performance. Parallel adders are used for fast binary addition which plays a crucial impersonation in majority of digital circuit designs including digital signal processors (DSP) and microprocessor data path unit. In this project we implement the parallel adder 32-bit SQRT CSLA(square root carry select adder) with BEC logic and compare them to the simple ripple carry adder(RCA),carry look ahead adder(CLA) & carry select adder(CSLA). To reduce the area and delay of n-bit CSLA, n-bit SQRT CSLA with BEC-1 logic was designed. Since CSLA is area consuming because it consists of dual RCA in structure. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. So as to achieve the same an efficient gate-level modification would be implemented to vitally reduce the delay of the CSLA. 32-bit SQRT CSLA with BEC-1logic is already designed which reduces the area of corresponding CSLA. But while performing area reduction and power reduction it is found that there is an increase in the delay. So in this project we put forward the structure of square root CSLA (SQRT CSLA) using "first addition logic circuit(FAL)" for 32-bit instead of BEC-1 logic circuit. The performance in terms of area, delay and utilization of power are calculated for SQRT CSLA with FAL and are compared with existing CSLA, SQRT CSLA and SQRT CSLA with BEC-1 logic.
References


Index Terms

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Keywords

Field programmable gate array (FPGA)  First addition logic (FAL)  Ripple carry Adder (RCA).