Abstract

In precursory efforts authors have illustriously consolidated the benefits of CPL based circuits and adiabatic logic conjoint the use of clock for even combinational blocks and reported the power diminution. With the adhibition of clock in combinational blocks, the same circuit topology may be employed for sequential behavior as manifested by authors in their erstwhile works. Proceeding forward in the same direction and augmenting another edge into this, authors have reported the reconfigurable circuit implementation utilizing the reported CPLAG concepts. In pursuance of the same authors have contemplated and implemented reconfigurable &apos;Nand&apos; and &apos;Nor&apos; gates. The same circuit topology can be used for either functionality governed by a control signal. The functional behavior of the circuit realized for &apos;Nand&apos; and &apos;Nor&apos; are analyzed and found to be cogent. The power results shows improvement by 4-5% as compared to SCMOS based circuits. The proposed RCPLAG universal gate is investigated for different voltage levels and transistor size. The parameters like power dissipation, power fed back to system, Trise, Tfall, propagation delays, PDP are further examined and found to be satisfactory. The best operating conditions for the said circuit lies in voltage range of less than 2.5V. The Pavg at 1V, 180nm technology is 12.2nW with 36f units PDP, 5µs maximum delay.
Reconfigurable CPL Adiabatic Gated Logic –RCPLAG based Universal NAND/NOR Gate

References

- Neil H. E. Weste and David Harris. CMOS VLSI Design: A Circuits and Systems Perspective. chapter 6, section 6. 2. 5. 2, Pearson, 236

Index Terms

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