Abstract

This paper enumerates the design of low power and high speed double edge triggered True Single Phase Clocking (TSPC) D- flip-flop. The TSPC CMOS flip-flop uses only one clock signal that is never inverted and it eliminates the clock skew. The originally developed TSPC flip-flop are very sensitive to the clock slope and large portion of power is spent in pre-charging the internal nodes, which makes TSPC dynamic circuits less power efficient. In the conventional CMOS design, high leakage current is becoming a significant contributor to power dissipation. To overcome the existing problem of CMOS TSPC D flip-flop, a Multi-threshold CMOS (MTCMOS) technology is used for leakage minimization. The designed flip-flops are compared in terms of power consumption and propagation delay and power delay product and simulations are carried out by MICROWIND 3.1 tools. The proposed MTCMOS designs such as original MTCMOS implementation and NMOS insertion in MTCMOS design of TSPC D flip-flop saves static power 57.517% and 58.871% as compared to conventional DE-TSPC D flip-flop respectively at 1.2V.
True Single Phase Clocking Flip-Flop Design using Multi Threshold CMOS Technique

- Jayanth Srinivasan, &quot;An Overview of Static Power Dissipation&quot;, CiteSeer public search engine and digital libraries for scientific and academic papers in the fields of computer and information science, pp. 1-7, 30 August 2011.

Index Terms

Computer Science

Circuits And Systems
Keywords
DE-TSPC flip-flop  MTCMOS  power dissipation  figure of merit (FOM)  BSIM.