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Abstract

Adders are the main components in digital designs which are used not only for addition but can be used for multiplication and division too. Adders find use in very large scale integrated circuits from processors (like in arithmetic logic circuits) to application specific integrated circuits. At the same time, high speed computation has become the important part of any digital applications today though low power is a key factor too. In this paper, a high speed full adder using improved differential split logic (DSL) technique is used. We further implement it in 1bit arithmetic logic circuit (ALU). Measurements show that proposed full adder is better than DSL full adder in terms of speed, and further implementation of it in ALU shows that it is better than CMOS ALU in terms of speed, power and power delay product (PDP).

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Index Terms

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Keywords

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