Abstract

In this paper a new SRAM cell is designed with a body bias controller to control leakage, speed and stability. A novel controller circuit is proposed to control the value of threshold voltage. Operation of the proposed controller is based on word line signal levels. In order to reduce sub threshold leakage current, the NMOS access and driver transistor is adjusted to a higher threshold voltage. Similarly, threshold voltage of NMOS access transistor is adjusted to a low value for improved read and writes speed. As compared to conventional 6T SRAM cell, the proposed design reduces the leakage power by about 52.27%, when tested on (8×16) SRAM cells.


**Index Terms**

Computer Science
Circuits And Systems

**Keywords**

Leakage Power Dissipation  Sub Threshold Current  Power Gating  Sleep Transistor And Transistor Stacking