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Abstract

In this paper a technique is proposed to reduce the leakage power of domino logic. In this proposed circuit pseudo dynamic buffer is used to reduce the power dissipation due to the precharge pulse propagation and leakage control transistor is used to reduce the leakage power. The leakage control transistors increase the resistance of the path from supply voltage to ground. As a result the leakage current is reduced. The cadence spectre tool at 180nm technology is used for simulation. The proposed logic is compared with the existing logic design. It is observed from the simulation that the power delay product and leakage current is reduced up to 32% and 10% respectively as compared to pseudo dynamic buffer based domino

logic.

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Keywords

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