Abstract

As per the present scenario every device as well as circuits are to be implemented with low power techniques so as to withstand the power challenges. In an arithmetic circuit multiplier who has much significant role in association with addition and subtraction process is also to be designed with low power technique so as to reduce the overall power consumption by the circuit. In this paper a four bit Braun multiplier is designed with different low power techniques and the main component of it i.e. the full adder design is modified and implemented with double gate MOSFET and the second important component i.e. the AND gate is designed with three different low power techniques. All the designs are compared on the basis of power,
Comparative Study of Different Low Power Designs of Braun Multiplier using Double Gate MOSFET at 45nm Technology

delay and power delay product (PDP). The designs are implemented in Cadence Virtuoso Tool with 45nm technology for its validation.

References


Index Terms

Computer Science
Circuits And Systems
Keywords
Braun Multiplier  Double Gate Mosfet  Sleepy Keeper  Pass Transistor Logic