Abstract

This paper presents the novel method to analyze and implement a full adder circuit using VHDL Technology. The results include successful compilation of the VHDL code in the Xilinx software along with the waveforms that prove the legality of the truth table. This paper also shows the effective use of Xilinx software in the analysis of the full adder circuit. It shows the Register Transfer Level (RTL) schematic diagrams and technology schematic diagrams of the different
VHDL architectural styles of modeling that include dataflow modeling, behavioral modeling and structural modeling. The analysis includes the detailed analysis of the fitter report and the timing report along with the synthesis report of the design summary. It also shows the chip floor plan of the full adder circuit.

References

- Chiuchisan, Potorac, 2010, Finite state machine design and VHDL coding techniques, 10th international conference on development and applications systems, Romania, PP-273-278.

Index Terms

Computational Science
Circuits And Systems

Keywords
Full Adder  Xilinx  Vhdl  Design.