Abstract

The IC technology always aims at increasing the package density and the speed. The VLSI technology which is governed by MOSFETs for the past couple of decades. In an attempt to increase the package density the size of the MOSFETS has been scaled down. As the size of the MOSFETs is scaled downwards, sub-threshold leakage current and leakage power in the ICs is increasing. The continued scaling has reached stagnation and further miniaturization of the MOSFET is facing major challenges. The conventional MOSFETs at short channel lengths suffer from high OFF-state leakage currents. They also suffer from numerous other short channel effects. Hence, as an alternative to the MOSFETs, TFETs have been widely studied. TFETs have the asymmetrical source/drain doping profile and they operate as reverse-biased,
gated p-i-n tunnel diodes. The on-off switching mechanism in TFETs can be achieved by the
gate-voltage induced band-to-band tunneling (BTBT) at the source-channel tunnel junction only.
Whereas in conventional MOSFETs, only the carriers with energy exceeding the
source-channel thermal barrier will contribute the on-state current. TFETs are promising
candidates for low power CMOS applications. Modelling the effects of non-idealities on the
drain current of a TFET is also an important aspect. High on-state current (I_{on}), high on-off
ratio and steep SS are the critical aspects in TFET design. In this paper the silvaco TCAD
simulation results for both conventional MOSFET & SOI Tunnel field effect transistor and its
structure are shown.

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**Index Terms**

Computer Science

Power System

**Keywords**

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