Abstract

Designing of reversible circuit has become the promising area for researchers. The designing
of digital circuits using reversible logic should have zero power loss in ideal conditions. However in practical aspect, it does not occur. This paper illustrates an optimized 8:1 multiplexer circuit grounded on reversible logic using a combination of available reversible logic gates. The multiplexer is optimized on the basis of two parameters namely total number of reversible gates used in the design of the circuits and total garbage outputs generated. This circuit is more advantageous for further designing of any digital circuit with low power loss. The devices designed through this circuit would have better performance as compared to the existing circuits.

References

- H. Thapliyal, M. B. Srinivas, "Novel Design and Reversible Logic Synthesis of
An Optimized Circuit of 8:1 Multiplexer Circuit using Reversible Logic Gates

Multiplexer Based Full Adder and Multipliers, IEEE, Vol. 2, pp. 1593-1596

Index Terms

Computer Science Circuits And System

Keywords

Reversible Circuit Design Basic Reversible Gates Multiplexer Circuit.