Abstract

In wide band communication systems, low power and high speed ADCs forms the main building blocks. These ADCs are commonly seen in the front end of the radio frequency receivers. Comparators are used in these ADCs. A CMOS Comparator design, based on amplifier-push pull inverter circuit is elaborated in this paper, which is intended to be used as the 1-bit ADC required for the implementation of a first order Delta Sigma (ΣΔ) A/D converter. This particular
Comparator Design for Delta Sigma Modulator

design for the comparator makes it faster and lowers the power dissipation. This design is
realized in both 180 nm and 90 nm CMOS processes using Cadence Virtuoso platform and low
power dissipation is found in 90 nm implementation with 1.2 V supply voltage. In this work
simulation results are reported and comparison of comparator in both technologies are
observed.

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Index Terms
Keywords
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