Abstract

Testing of Sequential circuits can be done by two test vectors (all 1's and all 0's) if the circuits were based on the conservative logic. The circuit is made to be tested by designing the circuit with the help of Reversible logic gates. Toffoli gate is used as reversible gate in this paper. Sequential circuits such as latches, flip flops are designed with the help of conservative logic reversible gate. Therefore, testing does not require any scan path access to the internal
memory cell since only normal mode and test mode are required for testing. Equivalent circuit of the Toffoli gate is presented which achieves the fault coverage. The objective of this paper is to reduce the number of test vectors. Fault coverage is also achieved rather than designing the circuit with fredkin gate. Power consumption may also reduce when compared with the fredkin gate.

References

- Himanshu Thapliyal and Nagarajan Ranganathan, "Design of reversible sequential circuits optimizing quantum cost, delay, and garbage outputs."  
- Himanshu Thapliyal, Nagarajan ranganathan, "Design of reversible sequential circuits optimizing quantum cost, delay, and garbage outputs".

**Index Terms**

Computer Science  
Circuits

**Keywords**

Conservative Logic  
Reversible Gate  
Fredkin Gate  
Toffoli Gate