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## Abstract

The aggressive technology scaling in the feature size has propelled the designers to integrate millions of transistors in a single die. Thus Multi-Processor System on Chip (MPSoC) has become the irrefutable elucidation to meet the demands of parallel computing in the domain of embedded systems. The gap between software development and actual hardware model has led to the emergence of virtual platforms so that the performance status can be improved even before the Register Transfer Logic (RTL) of the hardware is actualized. This paper presents a framework to bring accuracy to Open Virtual Platforms (OVP). Several architectures are modeled using this functional simulator and they are profiled to achieve a good accuracy/speed tradeoff. The accuracy of the simulation results is further enhanced by tuning profiling parameters and introducing an empirical correction factor which compensates the imprecisions of OVP that arise e. g. from missing simulated bus- and memory access times.

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### **Index Terms**

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### **Keywords**

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