Abstract

In general, multiplication plays an vital role in the development of processors, DSP applications, image processing etc. So, designing of high speed multiplier is a necessary choice. In this research, design of 4, 8 and 16-bit multiplier based on vedic mathematics has been presented. These multipliers further will be used in the design of convolutional encoder. Here, Urdhava Tiryakbhyam sutra is used for multiplication. It eliminates unwanted multiplication steps and
Design of 16-bit Vedic Multiplier for Convolutional Encoder using VHDL

follows a fast multiplication process and achieves a significantly less computation complexity over its conventional counterparts. All the modules are coded in VHDL and simulation done in Xilinx ISE 14.5i.

References


Index Terms

Computer Science
Circuits And Systems

Keywords

Convolution Encoder  Multiplier  Urdhava Tiryakbhyam  Vedic Mathematics