Performance Optimization of CP-PLL for SoC Applications

Abstract

Phase locked loops (PLLs) are integral parts of communication devices used in various applications such as frequency synthesizer, clock recovery circuits, synchronization for digital communications, carrier phase, frequency tracking, etc. The non-ideal effects in PLL such as jitter, phase noise, reference spurs, phase error, etc. influence the PLL performance which significantly affects the overall system. For example, a 10% performance degradation of PLL
leads to approximately 20% performance degradation of frequency synthesizers. In conventional CMOS charge pump circuit, phase error is caused due to leakage current, timing mismatch and current mismatch. The phase error due to current mismatch is more significant as compared to phase error due to timing mismatch and leakage current. Thus, in this work, two charge pump circuits with minimum area are designed in Matlab Simulink environment to reduce current mismatch. The designed charge pump using basic current mirror is compared with the ideal current mirror. Simulated results show that current mismatch and phase error for basic current mirror are approximately 12.19% and 0.3480 rad.

This setup can be easily utilized to design various charge pump to achieve minimum current mismatch for SoC applications.

References


Index Terms

Computer Science

Circuits And Systems
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Keywords
Charge Pump  Current Mismatch  Current Mirror  Design And Performance Of Charge Pump.