Abstract

In integrated circuits implemented to attain high value resistance, incremental resistance for both non-tunable, tunable pseudo-resistor has been estimated in Cadence Analog Design Environment using 0.18μm technology. Pseudo-resistors make use of diode-connected MOS devices working in subthreshold region and consume less area as compared to the discrete counterpart. Different V-R curves for both non-tunable and tunable pseudo-resistors are obtained and a comparison is presented in terms of linearity and consistency. Low tuning voltages, currents and smaller W/L ratios are selected for analysis to obtain high value resistors greater than 10¹¹Ω. It also leads to the design of low power integrated circuits.
References


Index Terms

Computer Science

Circuits And Systems
Keywords
Tunable Pseudo-resistors  Topologies  Integrated Circuits  Subthreshold Region.