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Abstract

This paper presents a comparative analysis of reduced segment; T and ? RLC interconnect models. With down scaling of technology, the interconnect structures have become a predominant factor in determining the overall circuit performance. Controlling interconnect propagation delay is the fundamental parameter to high speed VLSI designs. In this work, model performance has been evaluated in terms of propagation delay and power dissipation. The design models have been implemented using Cadence Virtuoso Analog Design Suite at 180nm CMOS technology at high frequency range of 0. 1GHz to 2GHz. A significant decrease of 38. 424ps in propagation delay has been observed in ?-Model as compared to the reduced

segment interconnect model. 7. 3253aW less power dissipation has been observed in reduced tree model when compared to RLC τ -Model.

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Computer Science

Index Terms

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Keywords

Interconnects; T-model; ?-model; Delay; Power Dissipation; Very Large Scale Integration (vlsi).