Abstract

Three valued logic which is also called as a ternary logic is a best alternative to conventional binary logic. Ternary logic has got its own importance due to its energy efficiency resulting from reduced complexity of interconnect and chip area. This paper presents a methodology for the design of ternary multiplexer circuit and also the design of ternary logic circuits based on CMOS. Designing of ternary multiplexer is presented first. Later the proposed methodology for the design of ternary logic circuits is presented. This proposed design methodology is used to
implement 1-bit half adder circuit using SPICE model. These new proposed implementations are compared with the old existing designs for the parameters like delay, power, number of transistors, power delay product etc. Simulation results indicate that the mux based 1-bit half adder design has reduced number of transistors, delay and power delay product when compared to the existing binary logic design.

References

- A Vertical Resonant Tunneling Transistor for Application in Digital Logic Circuits Jürgen Stock, Jörg Malindretos, Klaus Michael Indlekofer, Michael Pöttgens, Arno Förster, and Hans Lüth.

Index Terms

Computer Science Circuits And Systems
Keywords
Mosfet's  Ternary Logic  Ternary Multiplexer.