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Abstract

Physical design in VLSI circuits is getting more complex with increase in circuit complexity. The major troublesome job in physical design is the difficulties encountered in routing. In physical

design of digital circuits optimization of area is more important unlike in analog circuits where performance is given more priority. In the process of optimization of area in digital circuits routing in higher blocks can get more sophisticated. Standard cells are used as leaf cells in designing of higher digital blocks where the height of the standard cells has to be optimum. Therefore it is necessary to carefully design the standard cells and also create an environment for easy creation of bigger blocks using these leaf cells with simple routing at the top level. In this paper, a standard cell library is created where the height of the cells is optimized and also there are well defined space defined for systematic routing. Using these cells bigger digital blocks is created which demonstrates that routing can be made simple at the top level. In VLSI front end design parameters like gain, bandwidth, voltage swing etc are considered as major constraints [8]. In case of physical design of VLSI circuit's area, pin placement, routing, power planning and the shape of the layouts are the design constraints. In this paper, rectangular shapes for the leaf cells are created and the area of every standard cell is optimized. This helps in creation of digital circuits where one can access the created library and use the leaf cells as instance hence saving the design time. Routing is simplified by defining tracks on which metals will be routed. Tracks are designed such that any two metals can be routed on horizontal tracks placed one below other without the need to check of DRC rules. This is ensured by pre-defining the tracks and placing them at minimum DRC space defined by the technology used. All the digital circuits are implemented using cmos technology and the pmos and nmos devices widths are selected such that they are both of equal strength. This also ensures equal rise and fall time. All circuits are simulated using spectre tool and physical designs are verified for DRC and LVS.

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