Abstract

Arithmetic logic units and digital signal processors widely uses adders. It is the most complicated arithmetic circuits in digital electronics. The existing adders suffer from critical path delay, area overhead and power consumption. Speculative adders are designed with variable latency that combines speculation technique along with correction methodology to attain high performance in terms of low area overhead over the existing adders. In speculative adders the sum and carry generation part is separated to reduce the area overhead. Carry Speculative Adder (CSPA) uses carry predictor circuit to reduce power consumption and to reduce the computational time and it uses error recognition and error correction circuit to detect the fault
occurred in the partial sum generator and to recover it to get accurate results. CSPA circuit provides error free output so that it can be used in many digital applications. This speculative adder can reduce the delay upto 11.88%.

References


**Index Terms**

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**Keywords**

Speculative Adder  Variable Latency  Error Detection  Error Correction