Abstract

Placements of logical blocks in FPGA use many optimization algorithms in heuristic manner. Main objective is to provide minimization in wire length during the task placement inside Reconfigurable FPGAs, which will decrease the area, power and delay and increase the speed of execution. Optimization algorithms are applied in the Benchmark circuits and the results are compared. Due to the technological advancement, density of the devices increases so that necessitates improvement in minimization of wire length. Hence this project, proposes an optimum solution for wire length minimization.
Placement Compelled Steering Algorithm for Wire Length Minimization in FPGA

Keywords
Fpgas, Optimization Algorithm

Index Terms
Circuits And Systems

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