Abstract

A five stage current starved Voltage Controlled Oscillator (CMOS VCO) is designed in this paper. The design is implemented in Tanner environment with high oscillation frequency and low power consumption. Oscillation frequency of the designed VCO ranges from 25.70 MHz to 222.53 MHz. The circuit is simulated using 180nm SCN018 Technology. Simulation results reported that the power consumption is 58.47μA @ 1.8V VDD. Design procedures and simulation results are illustrated. This design is suitable for PLL as a frequency multiplier.
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- H. Cong, Simulations of Phase-Lock Loop in Communication Systems, College of Engineering, California State Polytechnic University, Pomona, CA.
- M. Suresh, Design of a Testable Jitter-Free Digital Phase-Locked Loop, Thesis (M.S.), Santa Clara University, School of Engineering, 1996.

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