Abstract

Implementation of low power techniques in the design is increasing because of the increasing clock frequency and a continuous increase in the number of transistors on chip. These low power techniques are being implemented across all levels of abstraction - system level to device level. Here, approaches related to front-end HDL based design styles, which can reduce power consumption, have been mentioned. As is known, power dissipation has a direct relation with the clock frequency and dynamic power also depends upon the rate at which the data toggles for a given circuit. The design styles mentioned here, focus on several areas of designing using HDL, which are at times not considered significant, as they do not affect the
functionality. The techniques mentioned here are quite simple to implement and mostly clear of confusion techniques that are considered quite insignificant, yet have a significant impact on the overall power-consumption.

References


Index Terms

Computer Science

Engineering and Technology

Keywords

RTL One-hot encoding Gray encoding Bus invert coding synthesis FSM