Abstract

The Least Mean Square Adaptive Filter is frequently encountered in wide variety of applications like signal processing, measurement and analysis of continuously changing parameters and signal analysis. The direct form of LMS Adaptive Filter does not support pipelining due to its recursive behavior. Thus modified Delayed LMS Adaptive Filter is preferred in which delays are decomposed so that pipelining is applied to power consuming blocks. Literature survey on the architectures of LMS Adaptive filter reveals that earlier works focused on the implementation using systolic architectures that gave rise to large adaptation delay. This arise a need for designing the LMS Adaptive filter with low adaptation delay. In this project, power efficient
A Ripple Carry Adder based Low Power Architecture of LMS Adaptive Filter

hardware architecture of modified delayed LMS Adaptive filter has been designed and implemented. The design of modified Delayed LMS Adaptive Filter is done after implementing pipelined architecture of Error Computation Block and Weight Update Block. The two important blocks involve the use of partial product generator and adder-tree structure which together perform the high-complexity operation. Adder-tree structure uses Carry-look ahead adder whose internal generate and propagate signals contribute to high power consumption. Hence further modification is made in the adder-tree structure by utilizing ripple-carry adder instead of carry-look ahead adder. This modification results in approximately 24% reduction in power relative to existing modified DLMS. Further power optimization is done by replacing adders with 4:2 compressors. The area complexity is also reduced as the number of required 4:2 compressors are less when compared to the requirement of adders. This modification results in 39% reduction in power relative to existing modified DLMS without degradation of steady-state-error performance. This implementation of power-optimized modified DLMS is done using Xilinx ISE Design Suite 14.2.

References

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Keywords
Delayed Least Mean Square (dlms) Adaptation Delay Power Optimization Pipelining.