Abstract

Embedded systems are mainly modeled by using Matlab's Simulink and Stateflow tools. Matlab's Simulink is a tool for modeling, simulating and analyzing software systems and Simulink Stateflow is a control logic tool used to model event-driven systems (Reactive systems) through state machines and flow charts within a Simulink model. In real time, systems undergo frequent changes, thus complexity of the systems grows and testing of the systems become time consuming and expensive even if changes occur in small parts of the system. So, these models need formal verification. In this paper, we focus on event-driven systems which are captured by Simulink Stateflow model. For this, we propose an algorithm generateFSM in which we first generate an XML file for the Simulink Stateflow model of a system. Then, we parse that XML file following top-down approach by using an XML parser. Next, we generate a
Generation of Test Cases based on Analysis of Simulink Stateflow Models

Finite State Machine (FSM) for the model, using the parsed information. By using this FSM, we generate test cases for the models of the embedded systems.

References


Index Terms

Computer Science

Software Engineering
Keywords
Simulink Tool  Simulink Stateflow Tool  Simulink Stateflow Model  Finite State Machine
(fsm)  Test Cases.