Abstract

The design approach of FFT algorithm for floating point numbers is investigated in this paper. Using Fast Fourier Transform (FFT), the Discrete Fourier Transform (DFT) can be implemented very fast. The FFT can be designed by radix-2 butterfly algorithm using Decimation in Time (DIT) or Decimation in Frequency (DIF) methods. Using IEEE-754 Single precision floating point and Double precision floating-point format the Fast Fourier Transform (FFT) for floating point numbers can be easily computed and simulated using VHDL tools. The floating point number can support a wide range of values. It can be represented using three fields: sign, exponent, and mantissa. The floating point Single precision format is always 32 bit and floating point Double...
precision format is always 64 bit. In this paper floating point addition, subtraction and multiplication algorithms is used. The IEEE-754 converter is used to convert decimal floating point number into Binary floating point format and it is also useful to verify the result. The floating point FFT processor reduce complexity of computation, area, delay and power consumption.

References

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Index Terms

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