Abstract

I am designing a 16 bit quaternary adder. Outline of the parallel rationale circuits is restricted by the necessity of the interconnections. A conceivable arrangement could be touched base at by utilizing a bigger arrangement of signs over the same chip region. Quaternary outlines are picking up significance from that point of view. It shows numerous esteemed full viper circuits, actualized in quaternary rationale. This is planned by utilizing one hot encoding and barrel shifter to accomplished Optimization in zone, speed and power will be accomplished by CMOS quaternary rationale. Sum and convey are handled in two separate squares, controlled by code generator unit. The circuit level execution of the different esteemed rationale administrators:
legitimate aggregate, consistent item, level-up, level-down and level transformations are exhibited. Plan check will be done by Tanner Tools.

References

- Amanda Das, Ifat Jahangir, Masud Hasan, Shafera Hossain "On Design And Analysis Of Quaternary Serial And Parallel Adder"; 978-1-4244-6890-4/10/$26. 00/2010 IEEE.

Index Terms

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