Abstract

Multi-Processor System on Chip (MPSoC) platforms are becoming increasingly more heterogeneous and are shifting towards a more communication-centric methodology. Networks on Chip (NoC) have emerged as the design paradigm for scalable on-chip communication architectures. As the system complexity grows, the problem emerges as how to design and instantiate such a NoC-based MPSoC platform in a systematic and automated way.

In this paper we present an integrated flow to automatically generate a highly configurable NoC-based MPSoC for FPGA instantiation. The system specification is done on a high level of abstraction, relieving the designer of error-prone and time consuming work. The flow uses the state-of-the-art Æthereal NoC, and Silicon Hive processing cores, both configurable at design- and run-time. We use this flow to generate a range of sample designs whose functionality has been verified on a Celoxica RC300E development board. The board, equipped with a Xilinx
Virtex II 6000, also offers a huge number of peripherals, and we show how their insertion is automated in the design for easy debugging and prototyping.

References

Design of Multinode Reconfigurable Network based Multiprocessor Systems on Chip

Index Terms

Computer Science

Circuits And Systems

Keywords

Multiprocessor  Multinode Reconfigurable Network  Network On Chip And Soc Mode