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## Abstract

Technology advances have made gigabit signal a viable and attractive. A method to design IEEE 1394 based 1GHz Phase Locked Loop (PLL) system as frequency synthesizer with Low Phase Noise is proposed. A complementary LC oscillator is used to generate the 1GHz oscillation frequency and is divided into lower frequency clock by the feedback frequency divider. The architecture is type II third order charge pump Phase Locked Loop. In order to suppress spurs and reduce ripples on control voltage a third order loop filter is used. Power consumption is significantly reduced by simplifying the circuit structure of digital frequency divider. Advance process of silicon-Germanium BiCMOS (SiGe) is used to integrate high-performance Hetero-junction Bipolar Transistors (HBTs) and MOSFETs actives and passives. This technology has the advantage that its flicker noise ( $1/f$ ) is very low.

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## Index Terms

Computer Science

Signal Processing

## Keywords

Phase Locked Loop Mixed Signal Simulation Vco Frequency Divider Passive Filter

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