Abstract

Low Power test pattern generator using a linear feedback shift register (LFSR), called LP-TGP
Low Power Test Pattern Generator for System on Chip Architecture

is presented to reduce the average and peak power of a circuit during test. The correlation between two test patterns generated by LP-TPG is more than between the random patterns. The goal of having intermediate patterns is to reduce the transitional activities of primary inputs which reduces the switching activities inside the circuit under test and hence power consumption. An experimental result shows that proposed method gives 30.87% reduction in power during testing.

References


Index Terms

Computer Science

Computing, Communication

And Sensor Network
Keywords
Built-in Self-test  Low Power  Single Input Pattern Testing  Switching Activity