Abstract

The advancement in technology has brought immense amount of changes in the design and productivity of applications designed for being used in the personal computers. By implementing greater number of cores to the same chip also results in facing challenges. In this case the challenge that is being faced is the core to core communication as well as the memory in addition to cache coherence. This paper presents a detailed analysis on performance of FFT
a divide and conquer algorithm across with the Multi-core architecture with Internal and external network. The architectures are being defined using memory configuration and context configuration with help of Multi2Sim 3.4 simulator. The performance of these architectures have been simulated with Splash 2 Benchmark.

References

- D. Pham et al, "The Design and Implementation of a First-Generation CELL Processor", ISSCC.
- D. Geer, "For Programmers, Multi-core Chips Mean Multiple Challenges", Computer, September 2007.
- D. Stasiak et al, "Cell Processor Low-Power Design Methodology", IEEE Micro, September 2005
- W. Knight, "Two Heads are better than One", IEEE Review, September 2005
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- Zhongliang Chan et al, "The Multi2Sim Simulation Framework".

Index Terms

Computer Science  Computing, Communication

And Sensor Network

Keywords

Multi-core Technology  Multi-core Issues  Splash2 Benchmark  Performance  Multi2sim Simulator