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Abstract

Process variation is considered to be a major concern in the design of circuits including interconnect pipelines in current deep submicron regime. Process variation results in uncertainties of circuit performances such as propagation delay. The performance of VLSI/ULSI chip is becoming less predictable as device dimensions shrinks below the sub-100-nm scale. The reduced predictability can be attributed to poor control of the physical features of devices and interconnects during the manufacturing process. Variations in these quantities maps to variations in the electrical behavior of circuits. The interconnect line resistance and capacitance varies due to changes in interconnect width and thickness, substrate, implant impurity level, and

surface charge. This paper provides an analysis of the effect of interconnect parasitic variation on the propagation delay through driver-interconnect-load (DIL) system. The impact of process induced variations on propagation delay of the circuit is discussed for three different fabrication technologies i.e. 130nm, 70nm and 45nm. The comparison between three technologies interestingly shows that the effect of line resistive and capacitive parasitic variation on propagation delay has almost uniform trend as feature size shrinks. However, resistive parasitic variation in global interconnects has very nominal effect on the propagation delay as compared to capacitive parasitic. Propagation delay variation is from 0.01% to 0.04% and -4.32% to 18.1 % due to resistive and capacitive deviation of -6.1% to 25% respectively.

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Index Terms

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Key words

Process variation

parasitic

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driver

load

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