Abstract

Network-on-Chip (NoC) has been proposed as a solution for addressing the communication infrastructure design challenges of future high-performance nanoscale architecture of SoCs. IrNIRGAM is a discrete event, cycle accurate simulator targeted at irregular topology based Network on Chip (NoC) research. The generic, modular, and extensible framework of IrNIRGAM provides substantial support to experiment with direct network based NoC designs in terms of routing algorithms, applications on various topologies and related performance parameters such as throughput, communication latency etc. IrNIRGAM is written in SystemC and C++. Topology represents the most important characteristic of NoC architectures and essentially defines the
physical interconnection of the router nodes. In IrNIRGAM, input buffered routers can have multiple virtual channels (VCs) and uses wormhole switching for flow control. The packets are split into an arbitrary number of flits (flow control units) and forwarded through the network in a pipelined fashion. A Round-Robin scheme for switch arbitration is used in the router nodes to provide fair bandwidth allocation while effectively preventing scheduling anomalies like starvation.

Reference

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Index Terms

Computer Science Communications

Key words

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Network-on-Chip Simulation

IP Core

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