Abstract

Modified decoding algorithms for DS codes are proposed that, in addition to error correction, provide error detection when the number of correctable bit errors is exceeded by one. This combined error detection and correction capability of the modified decoder are provide to prevent soft errors from causing data corruption, memories are typically protected with error correction codes (ECCs). Memory applications require low latency encoders and decoders. These codes allow us to design a fault tolerant error-detector unit that detects any error in the received code-vector despite having faults in the detector circuitry. The fault secure detector unit to check the output vector of the encoder and corrector circuitry, and if there is any error in
the output of either of these units, that unit has to redo the operation to generate the correct output vector. Using this detect-and-repeat technique, correct potential transient errors in the encoder or corrector output and provide fault tolerant memory system with fault-tolerant supporting circuitry.

References

- Efficient Majority Logic Fault Detection With Difference-Set Codes for Memory Applications Shih-Fu Liu, Pedro Reviriego, Member, IEEE, and Juan Antonio Maestro, Member, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 20, NO. 1, JANUARY 2012

Index Terms
Fault Secure Memory Design using Difference Set Codes

Keywords
Error Correction Codes  Low-density Parity Check (ldpc)  Memory  Majority Logic